



# Complete Quad, 16-Bit, High Accuracy, Serial Input, Bipolar Voltage Output DACs

## AD5764

### FEATURES

- Complete quad, 16-bit digital-to-analog converters (DACs)
- Programmable output range  
 $\pm 10\text{ V}$ ,  $\pm 10.2564\text{ V}$ , or  $\pm 10.5263\text{ V}$
- $\pm 1\text{ LSB}$  maximum INL error,  $\pm 1\text{ LSB}$  maximum DNL error
- Low noise:  $60\text{ nV}/\sqrt{\text{Hz}}$
- Settling time:  $10\text{ }\mu\text{s}$  maximum
- Integrated reference buffers
- Output control during power-up/brownout
- Programmable short-circuit protection
- Simultaneous updating via LDAC
- Asynchronous CLR to zero code
- Digital offset and gain adjust
- Logic output control pins
- DSP-/microcontroller-compatible serial interface
- Temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- iCMOS process technology<sup>1</sup>

### APPLICATIONS

- Industrial automation
- Open-/closed-loop servo control
- Process control
- Data acquisition systems
- Automatic test equipment
- Automotive test and measurement
- High accuracy instrumentation

### GENERAL DESCRIPTION

The AD5764 is a quad, 16-bit, serial input, bipolar voltage output DAC that operates from supply voltages of  $\pm 11.4\text{ V}$  to  $\pm 16.5\text{ V}$ . Nominal full-scale output range is  $\pm 10\text{ V}$ . The AD5764 provides integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry. The part also features a digital I/O port, which is programmed via the serial interface. The part incorporates digital offset and gain adjust registers per channel.

The AD5764 is a high performance converter that offers guaranteed monotonicity, integral nonlinearity (INL) of  $\pm 1\text{ LSB}$ , low noise, and  $10\text{ }\mu\text{s}$  settling time. During power-up (when the supply voltages are changing),  $\text{VOUTx}$  is clamped to  $0\text{ V}$  via a low impedance path.

The AD5764 uses a serial interface that operates at clock rates of up to  $30\text{ MHz}$  and is compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is programmable to either twos complement or offset binary formats. The asynchronous clear function clears all DAC registers to either bipolar zero or zero scale depending on the coding used. The AD5764 is ideal for both closed-loop servo control and open-loop control applications. The AD5764 is available in a 32-lead TQFP, and offers guaranteed specifications over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  industrial temperature range. See Figure 1 for functional block diagram.

Table 1. Related Devices

Part No.	Description
AD5764R	AD5764 with internal voltage reference
AD5744	Complete quad, 14-bit, high accuracy, serial input, bipolar voltage output DAC
AD5744R	AD5744 with internal voltage reference

<sup>1</sup> For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher voltage levels, iCMOS® is a technology platform that enables the development of analog ICs capable of  $30\text{ V}$  and operating at  $\pm 15\text{ V}$  supplies, allowing dramatic reductions in power consumption and package size, and increased ac and dc performance.

### Rev. B

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## REVISION HISTORY

### 05/08—Rev. A to Rev. B

Changes to Table Summary Statement, Specifications Section..	4
Changes to Power Requirements Parameter, Table 2 and Table Summary Statement.....	5
Changes to $t_{16}$ Parameter, Table 4.....	6
Changes to Table 6.....	10
Changed $V_{SS}/V_{DD}$ to $AV_{SS}/AV_{DD}$ in Typical Performance Characteristics Section.....	13
Changes to Table 16.....	22
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### 1/07—Rev. 0 to Rev. A

Changes to Absolute Maximum Ratings .....	10
Changes to Figure 25 and Figure 26.....	16

### 3/06—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

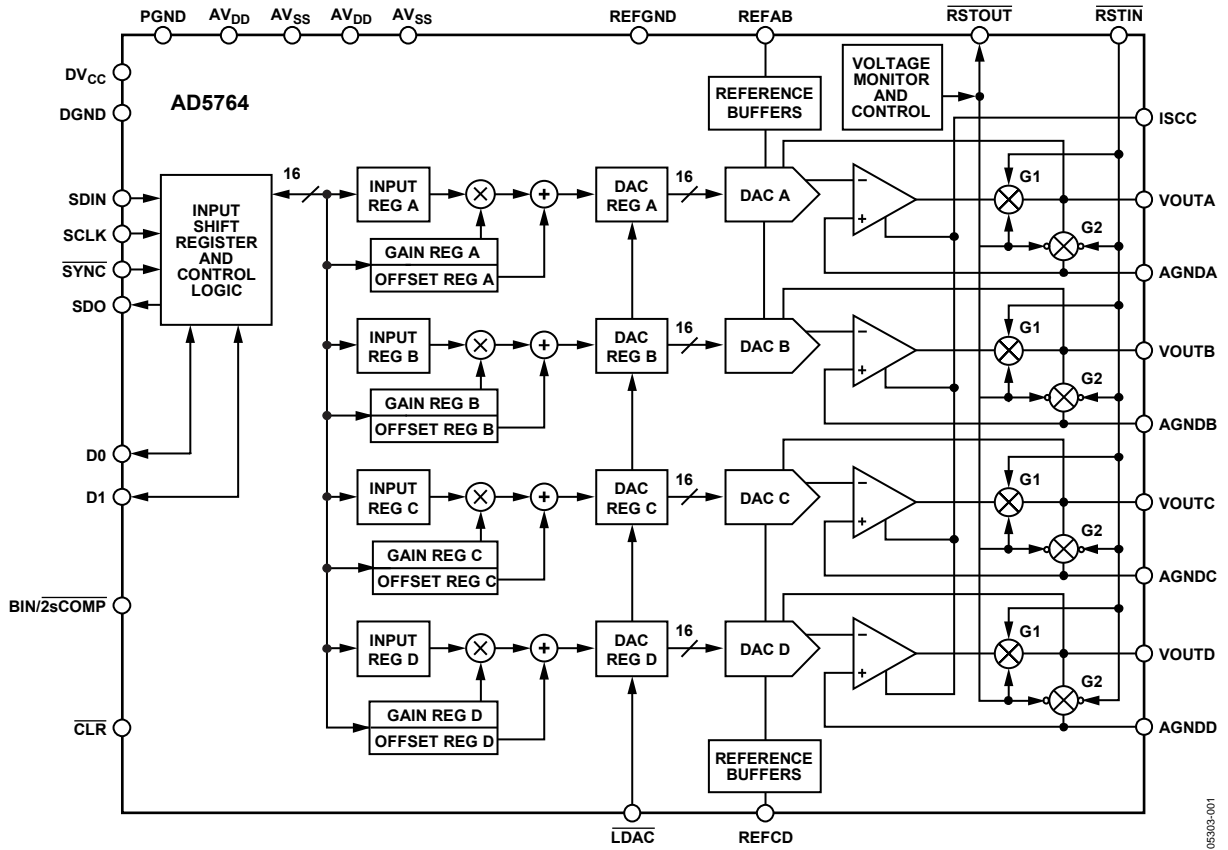


Figure 1.

05303-001

## SPECIFICATIONS

$AV_{DD} = 11.4\text{ V to }16.5\text{ V}$ ,  $AV_{SS} = -11.4\text{ V to }-16.5\text{ V}$ ,  $AGND_x = DGND = REFGND = PGND = 0\text{ V}$ ;  $REFAB = REFCD = 5\text{ V}$ ;  $DV_{CC} = 2.7\text{ V to }5.25\text{ V}$ ,  $R_{LOAD} = 10\text{ k}\Omega$ ,  $C_L = 200\text{ pF}$ . Temperature range:  $-40^\circ\text{C to }+85^\circ\text{C}$ ; typical at  $+25^\circ\text{C}$ . Device functionality is guaranteed to  $+105^\circ\text{C}$  with degraded performance. All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 2.**

Parameter	A Grade	B Grade	C Grade	Unit	Test Conditions/Comments
<b>ACCURACY</b>					Outputs unloaded
Resolution	16	16	16	Bits	
Relative Accuracy (INL)	$\pm 4$	$\pm 2$	$\pm 1$	LSB max	
Differential Nonlinearity	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	Guaranteed monotonic
Bipolar Zero Error	$\pm 2$	$\pm 2$	$\pm 2$	mV max	At $25^\circ\text{C}$ ; error at other temperatures obtained using bipolar zero TC
Bipolar Zero Temperature Coefficient (TC) <sup>1</sup>	$\pm 2$	$\pm 2$	$\pm 2$	ppm FSR/ $^\circ\text{C}$ max	
Zero-Scale Error	$\pm 2$	$\pm 2$	$\pm 2$	mV max	At $25^\circ\text{C}$ ; error at other temperatures obtained using zero-scale TC
Zero-Scale TC <sup>1</sup>	$\pm 2$	$\pm 2$	$\pm 2$	ppm FSR/ $^\circ\text{C}$ max	
Gain Error	$\pm 0.02$	$\pm 0.02$	$\pm 0.02$	% FSR max	At $25^\circ\text{C}$ ; error at other temperatures obtained using gain TC
Gain TC <sup>1</sup>	$\pm 2$	$\pm 2$	$\pm 2$	ppm FSR/ $^\circ\text{C}$ max	
DC Crosstalk <sup>1</sup>	0.5	0.5	0.5	LSB max	
<b>REFERENCE INPUT<sup>1</sup></b>					
Reference Input Voltage	5	5	5	V nominal	$\pm 1\%$ for specified performance
DC Input Impedance	1	1	1	M $\Omega$ min	Typically 100 M $\Omega$
Input Current	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	Typically $\pm 30\text{ nA}$
Reference Range	1 to 7	1 to 7	1 to 7	V min to V max	
<b>OUTPUT CHARACTERISTICS<sup>1</sup></b>					
Output Voltage Range <sup>2</sup>	$\pm 10.5263$	$\pm 10.5263$	$\pm 10.5263$	V min to V max	$AV_{DD}/AV_{SS} = \pm 11.4\text{ V}$ , $REFIN = 5\text{ V}$
	$\pm 14$	$\pm 14$	$\pm 14$	V min to V max	$AV_{DD}/AV_{SS} = \pm 16.5\text{ V}$ , $REFIN = 7\text{ V}$
Output Voltage Drift vs. Time	$\pm 13$	$\pm 13$	$\pm 13$	ppm FSR/500 hours typ	
	$\pm 15$	$\pm 15$	$\pm 15$	ppm FSR/1000 hours typ	
Short-Circuit Current	10	10	10	mA typ	$R_{ISCC} = 6\text{ k}\Omega$ , see Figure 31
Load Current	$\pm 1$	$\pm 1$	$\pm 1$	mA max	For specified performance
Capacitive Load Stability					
$R_{LOAD} = \infty$	200	200	200	pF max	
$R_{LOAD} = 10\text{ k}\Omega$	1000	1000	1000	pF max	
DC Output Impedance	0.3	0.3	0.3	$\Omega$ max	
<b>DIGITAL INPUTS<sup>1</sup></b>					$DV_{CC} = 2.7\text{ V to }5.25\text{ V}$ , JEDEC compliant
Input High Voltage, $V_{IH}$	2	2	2	V min	
Input Low Voltage, $V_{IL}$	0.8	0.8	0.8	V max	
Input Current	$\pm 1$	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	Per pin
Pin Capacitance	10	10	10	pF max	Per pin

Parameter	A Grade	B Grade	C Grade	Unit	Test Conditions/Comments
<b>DIGITAL OUTPUTS (D0, D1, SDO)<sup>1</sup></b>					
Output Low Voltage	0.4	0.4	0.4	V max	DV <sub>CC</sub> = 5 V ± 5%, sinking 200 μA
Output High Voltage	DV <sub>CC</sub> - 1	DV <sub>CC</sub> - 1	DV <sub>CC</sub> - 1	V min	DV <sub>CC</sub> = 5 V ± 5%, sourcing 200 μA
Output Low Voltage	0.4	0.4	0.4	V max	DV <sub>CC</sub> = 2.7 V to 3.6 V, sinking 200 μA
Output High Voltage	DV <sub>CC</sub> - 0.5	DV <sub>CC</sub> - 0.5	DV <sub>CC</sub> - 0.5	V min	DV <sub>CC</sub> = 2.7 V to 3.6 V, sourcing 200 μA
High Impedance Leakage Current	±1	±1	±1	μA max	SDO only
High Impedance Output Capacitance	5	5	5	pF typ	SDO only
<b>POWER REQUIREMENTS</b>					
AV <sub>DD</sub> /AV <sub>SS</sub>	±11.4 to ±16.5	±11.4 to ±16.5	±11.4 to ±16.5	V min to V max	
DV <sub>CC</sub>	2.7 to 5.25	2.7 to 5.25	2.7 to 5.25	V min to V max	
Power Supply Sensitivity <sup>1</sup>					
ΔV <sub>OUT</sub> /ΔAV <sub>DD</sub>	-85	-85	-85	dB typ	
AI <sub>DD</sub>	3.5	3.5	3.5	mA/channel max	Outputs unloaded
AI <sub>SS</sub>	2.75	2.75	2.75	mA/channel max	Outputs unloaded
DI <sub>CC</sub>	1.2	1.2	1.2	mA max	V <sub>H</sub> = DV <sub>CC</sub> , V <sub>IL</sub> = DGND, 750 μA typical
Power Dissipation	275	275	275	mW typ	±12 V operation output unloaded

<sup>1</sup> Guaranteed by design and characterization; not production tested.

<sup>2</sup> Output amplifier headroom requirement is 1.4 V minimum.

### AC PERFORMANCE CHARACTERISTICS

AV<sub>DD</sub> = 11.4 V to 16.5 V, AV<sub>SS</sub> = -11.4 V to -16.5 V, AGND<sub>x</sub> = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V;

DV<sub>CC</sub> = 2.7 V to 5.25 V, R<sub>LOAD</sub> = 10 kΩ, C<sub>L</sub> = 200 pF. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

**Table 3.**

Parameter	A Grade	B Grade	C Grade	Unit	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE<sup>1</sup></b>					
Output Voltage Settling Time	8	8	8	μs typ	Full-scale step to ±1 LSB
	10	10	10	μs max	
	2	2	2	μs typ	
Slew Rate	5	5	5	V/μs typ	512 LSB step settling
Digital-to-Analog Glitch Energy	8	8	8	nV-sec typ	
Glitch Impulse Peak Amplitude	25	25	25	mV max	
Channel-to-Channel Isolation	80	80	80	dB typ	
DAC-to-DAC Crosstalk	8	8	8	nV-sec typ	
Digital Crosstalk	2	2	2	nV-sec typ	
Digital Feedthrough	2	2	2	nV-sec typ	Effect of input bus activity on DAC outputs
Output Noise (0.1 Hz to 10 Hz)	0.1	0.1	0.1	LSB p-p typ	
Output Noise (0.1 Hz to 100 kHz)	45	45	45	μV rms max	
1/f Corner Frequency	1	1	1	kHz typ	
Output Noise Spectral Density	60	60	60	nV/√Hz typ	Measured at 10 kHz
Complete System Output Noise Spectral Density <sup>2</sup>	80	80	80	nV/√Hz typ	Measured at 10 kHz

<sup>1</sup> Guaranteed by design and characterization; not production tested.

<sup>2</sup> Includes noise contributions from integrated reference buffers, 16-bit DAC and output amplifier.

# AD5764

## TIMING CHARACTERISTICS

$AV_{DD} = 11.4\text{ V to }16.5\text{ V}$ ,  $AV_{SS} = -11.4\text{ V to }-16.5\text{ V}$ ,  $AGND_x = DGND = REFGND = PGND = 0\text{ V}$ ;  $REFAB = REFCD = 5\text{ V}$ ;  $DV_{CC} = 2.7\text{ V to }5.25\text{ V}$ ,  $R_{LOAD} = 10\text{ k}\Omega$ ,  $C_L = 200\text{ pF}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 4.

Parameter <sup>1, 2, 3</sup>	Limit at $T_{MIN}, T_{MAX}$	Unit	Description
$t_1$	33	ns min	SCLK cycle time
$t_2$	13	ns min	SCLK high time
$t_3$	13	ns min	SCLK low time
$t_4$	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
$t_5^4$	13	ns min	24 <sup>th</sup> SCLK falling edge to $\overline{SYNC}$ rising edge
$t_6$	40	ns min	Minimum $\overline{SYNC}$ high time
$t_7$	2	ns min	Data setup time
$t_8$	5	ns min	Data hold time
$t_9$	1.4	$\mu\text{s min}$	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated)
	400	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
$t_{10}$	10	ns min	$\overline{LDAC}$ pulse width low
$t_{11}$	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
$t_{12}$	10	$\mu\text{s max}$	DAC output settling time
$t_{13}$	10	ns min	$\overline{CLR}$ pulse width low
$t_{14}$	2	$\mu\text{s max}$	$\overline{CLR}$ pulse activation time
$t_{15}^{5, 6}$	25	ns max	SCLK rising edge to SDO valid
$t_{16}$	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
$t_{17}$	2	$\mu\text{s min}$	$\overline{SYNC}$ rising edge to DAC output response time ( $\overline{LDAC} = 0$ )
$t_{18}$	170	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge

<sup>1</sup> Guaranteed by design and characterization; not production tested.

<sup>2</sup> All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of  $DV_{CC}$ ) and timed from a voltage level of 1.2 V.

<sup>3</sup> See Figure 2, Figure 3, and Figure 4.

<sup>4</sup> Standalone mode only.

<sup>5</sup> Measured with the load circuit of Figure 5.

<sup>6</sup> Daisy-chain mode only.

Timing Diagrams

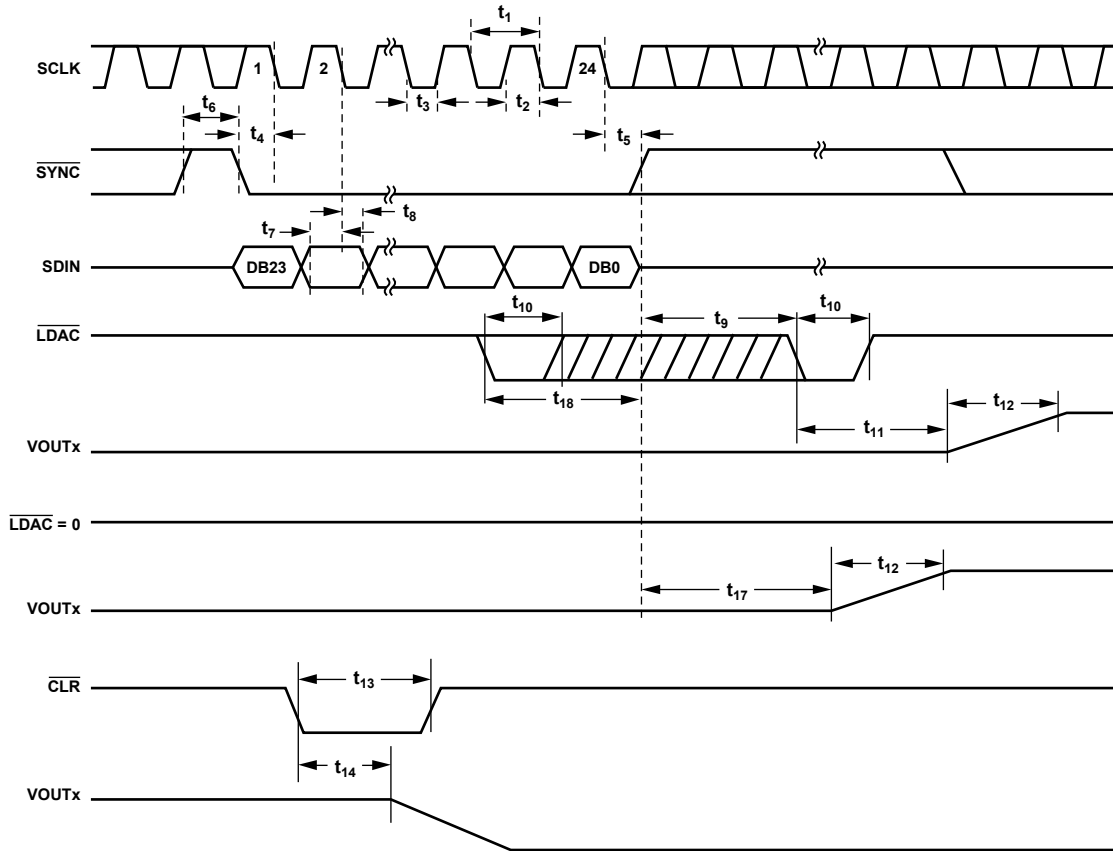


Figure 2. Serial Interface Timing Diagram

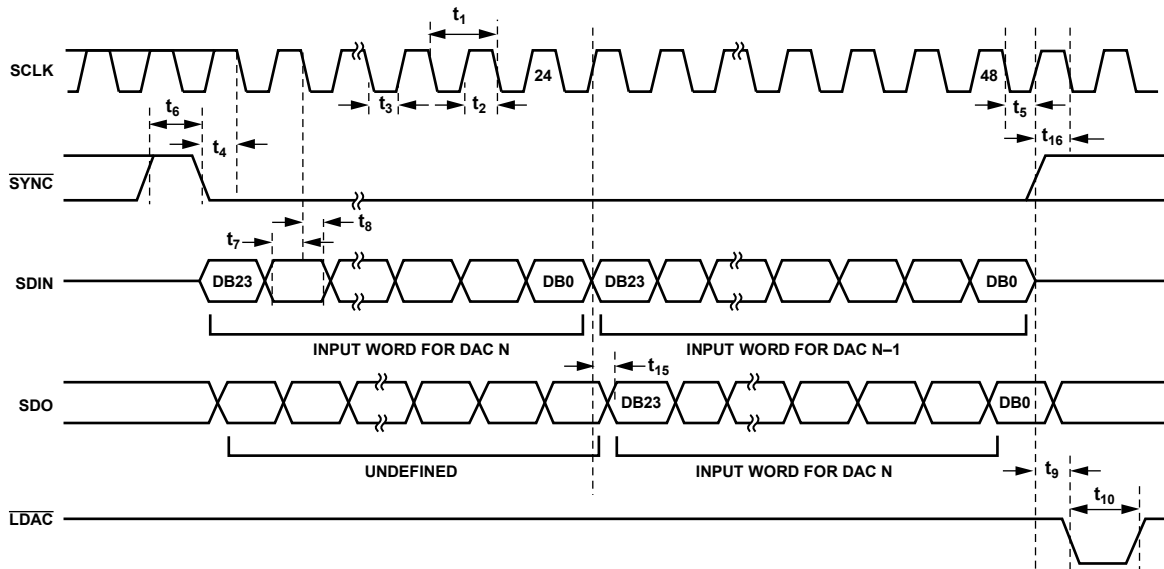
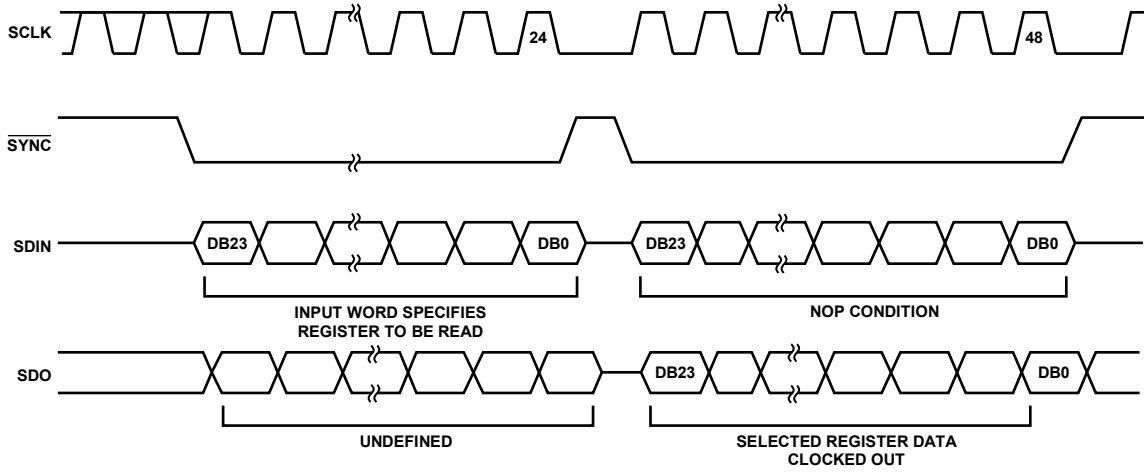
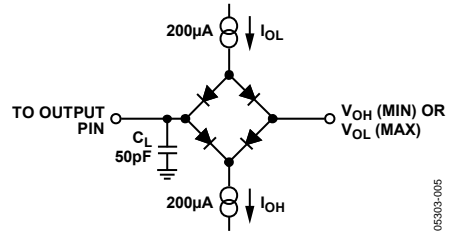


Figure 3. Daisy-Chain Timing Diagram



05303-004

Figure 4. Readback Timing Diagram



05303-005

Figure 5. Load Circuit for SDO Timing Diagram



## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
$AV_{DD}$ to AGNDx, DGND	-0.3 V to +17 V
$AV_{SS}$ to AGNDx, DGND	+0.3 V to -17 V
$DV_{CC}$ to DGND	-0.3 V to +7 V
Digital Inputs to DGND	-0.3 V to $DV_{CC} + 0.3$ V or 7 V (whichever is less)
Digital Outputs to DGND	-0.3 V to $DV_{CC} + 0.3$ V
REFIN to AGNDx, PGND	-0.3 V to $AV_{DD} + 0.3$ V
VOUTA, VOUTB, VOUTC, VOUTD to AGNDx	$AV_{SS}$ to $AV_{DD}$
AGNDx to DGND	-0.3 V to +0.3 V
Operating Temperature Range Industrial	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_J$ max)	150°C
32-Lead TQFP	
$\theta_{JA}$ Thermal Impedance	65°C/W
$\theta_{JC}$ Thermal Impedance	12°C/W
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

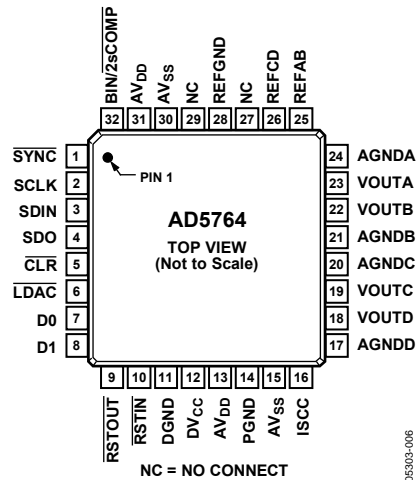


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC	Active Low Input. This is the frame synchronization signal for the serial interface. While SYNC is low, data is transferred in on the falling edge of SCLK.
2	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
3	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode.
5 <sup>1</sup>	CLR	Negative Edge Triggered Input. Asserting this pin sets the DAC registers to 0x0000.
6	LDAC	Load DAC. Logic input. This is used to update the DAC registers and consequently the analog outputs. When tied permanently low, the addressed DAC register is updated on the rising edge of SYNC. If LDAC is held high during the write cycle, the DAC input register is updated but the output update is held off until the falling edge of LDAC. In this mode, all analog outputs can be updated simultaneously on the falling edge of LDAC. The LDAC pin must not be left unconnected.
7, 8	D0, D1	Digital I/O port. The user can set up these pins as inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, these pins have weak internal pull-ups to DV <sub>CC</sub> . When programmed as outputs, D0 and D1 are referenced by DV <sub>CC</sub> and DGND.
9	RSTOUT	Reset Logic Output. This is the output from the on-chip voltage monitor used in the reset circuit. If desired, it can be used to control other system components.
10	RSTIN	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, RSTIN should be tied to Logic 1. Register values remain unchanged.
11	DGND	Digital Ground Pin.
12	DV <sub>CC</sub>	Digital Supply Pin. Voltage ranges from 2.7 V to 5.25 V.
13, 31	AV <sub>DD</sub>	Positive Analog Supply Pins. Voltage ranges from 11.4 V to 16.5 V.
14	PGND	Ground Reference Point for Analog Circuitry.
15, 30	AV <sub>SS</sub>	Negative Analog Supply Pins. Voltage ranges from -11.4 V to -16.5 V.
16	ISCC	Resistor Connection for Pin Programmable Short-Circuit Current. This pin is used in association with an optional external resistor to AGND to program the short-circuit current of the output amplifiers. Refer to the Design Features section for further details.
17	AGNDD	Ground Reference Pin for DAC D Output Amplifier.
18	VOUTD	Analog Output Voltage of DAC D. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
19	VOUTC	Analog Output Voltage of DAC C. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
20	AGNDC	Ground Reference Pin for DAC C Output Amplifier.
21	AGNDB	Ground Reference Pin for DAC B Output Amplifier.

Pin No.	Mnemonic	Description
22	VOUTB	Analog Output Voltage of DAC B. Buffered output with a nominal full-scale output range of $\pm 10$ V. The output amplifier is capable of directly driving a 10 k $\Omega$ , 200 pF load.
23	VOUTA	Analog Output Voltage of DAC A. Buffered output with a nominal full-scale output range of $\pm 10$ V. The output amplifier is capable of directly driving a 10 k $\Omega$ , 200 pF load.
24	AGNDA	Ground Reference Pin for DAC A Output Amplifier.
25	REFAB	External Reference Voltage Input for Channel A and Channel B. Reference input range is 1 V to 7 V; programs the full-scale output voltage. REFIN = 5 V for specified performance.
26	REFCD	External Reference Voltage Input for Channel C and Channel D. Reference input range is 1 V to 7 V; programs the full-scale output voltage. REFIN = 5 V for specified performance.
27, 29	NC	No Connect.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
32	BIN/ <u>2sCOMP</u>	Determines the DAC Coding. This pin should be hardwired to either DV <sub>CC</sub> or DGND. When hardwired to DV <sub>CC</sub> , input coding is offset binary. When hardwired to DGND, input coding is twos complement (see Table 7).

<sup>1</sup> Internal pull-up device on this logic input. Therefore, it can be left floating and defaults to a Logic 1 condition.

TYPICAL PERFORMANCE CHARACTERISTICS

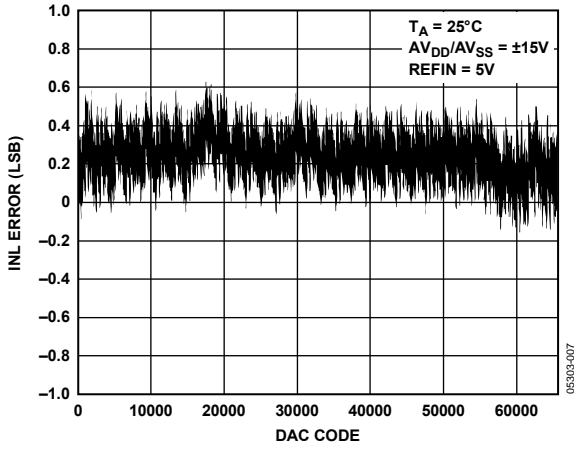


Figure 7. Integral Nonlinearity Error vs. Code,  $AV_{DD}/AV_{SS} = \pm 15 V$

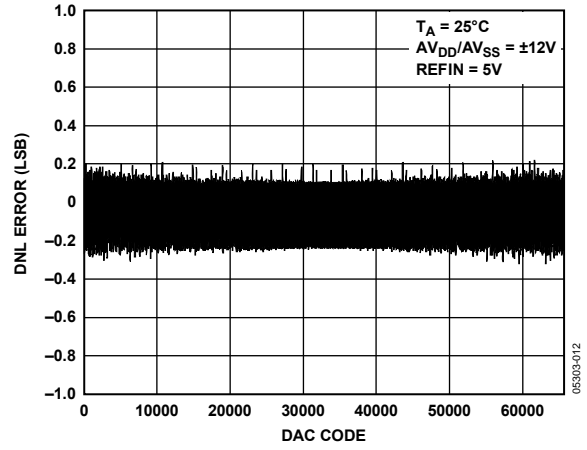


Figure 10. Differential Nonlinearity Error vs. Code,  $AV_{DD}/AV_{SS} = \pm 12 V$

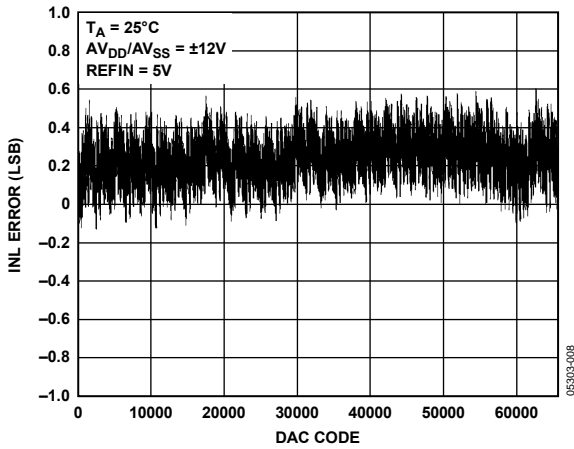


Figure 8. Integral Nonlinearity Error vs. Code,  $AV_{DD}/AV_{SS} = \pm 12 V$

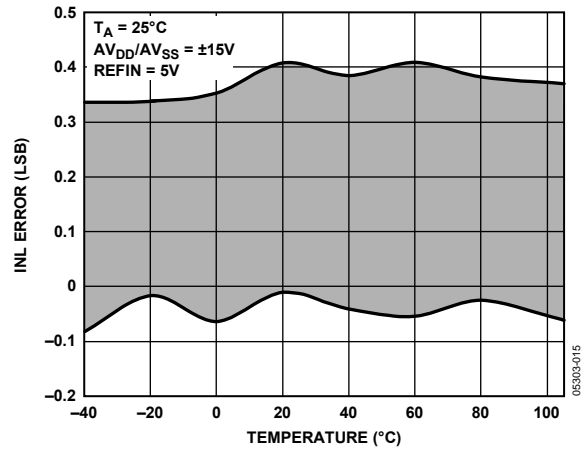


Figure 11. Integral Nonlinearity Error vs. Temperature,  $AV_{DD}/AV_{SS} = \pm 15 V$

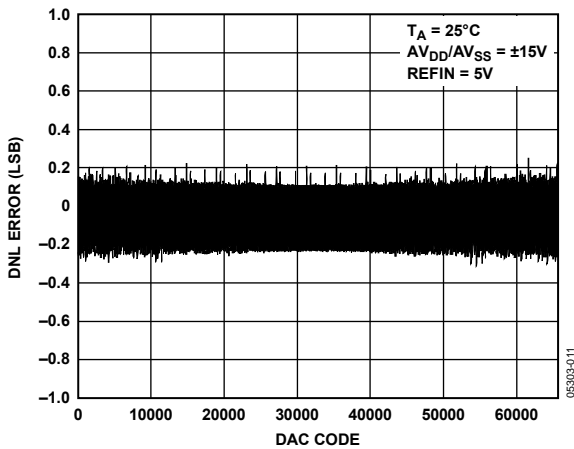


Figure 9. Differential Nonlinearity Error vs. Code,  $AV_{DD}/AV_{SS} = \pm 15 V$

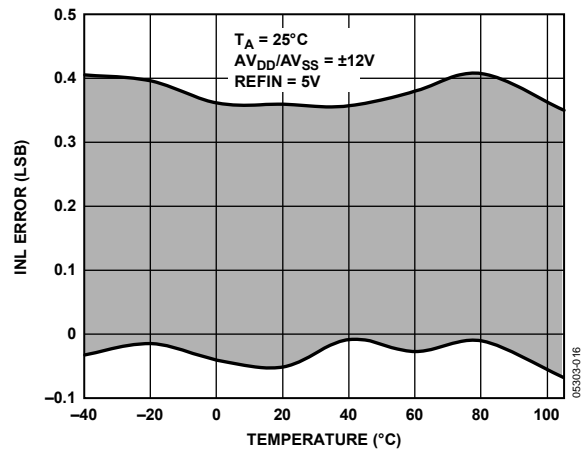


Figure 12. Integral Nonlinearity Error vs. Temperature,  $AV_{DD}/AV_{SS} = \pm 12 V$

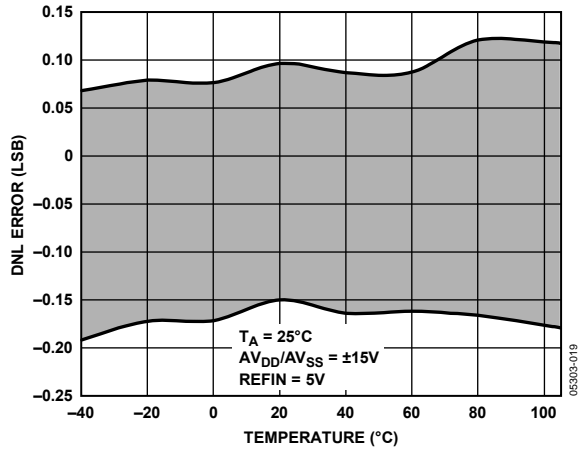


Figure 13. Differential Nonlinearity Error vs. Temperature,  $AV_{DD}/AV_{SS} = \pm 15V$

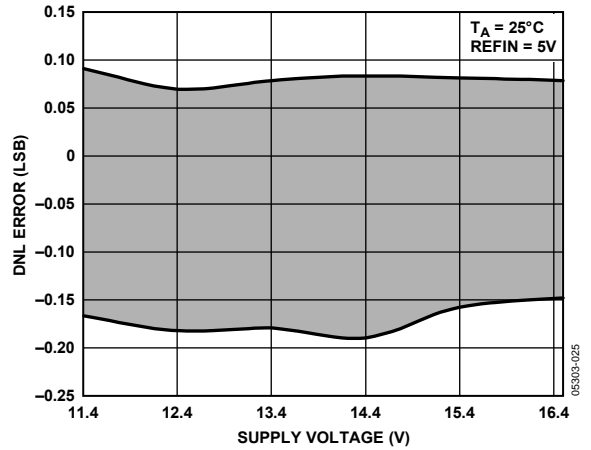


Figure 16. Differential Nonlinearity Error vs. Supply Voltage

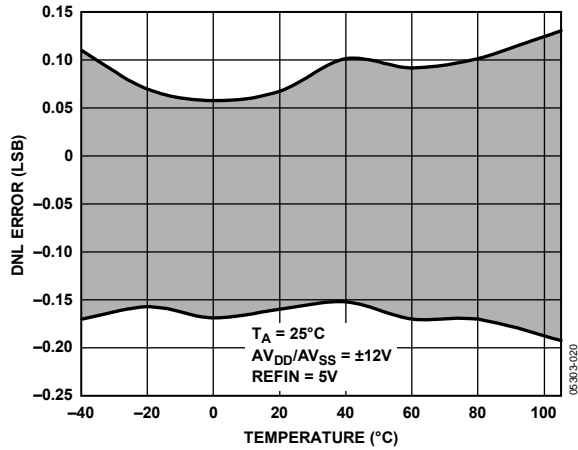


Figure 14. Differential Nonlinearity Error vs. Temperature,  $AV_{DD}/AV_{SS} = \pm 12V$

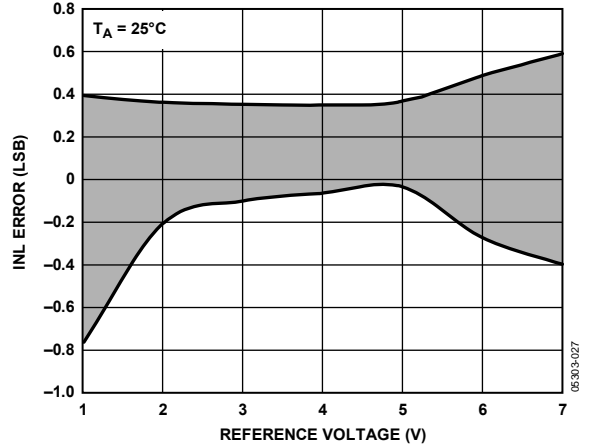


Figure 17. Integral Nonlinearity Error vs. Reference Voltage,  $AV_{DD}/AV_{SS} = \pm 16.5V$

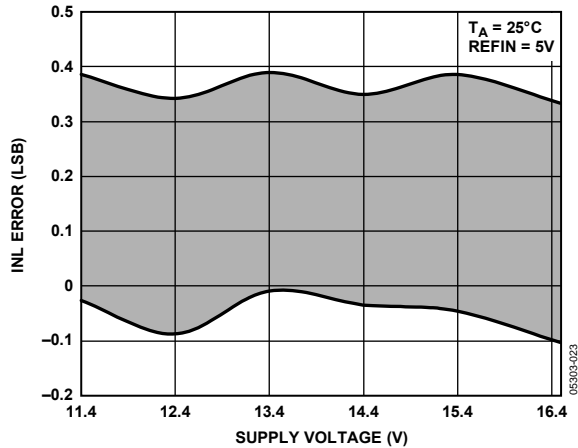


Figure 15. Integral Nonlinearity Error vs. Supply Voltage

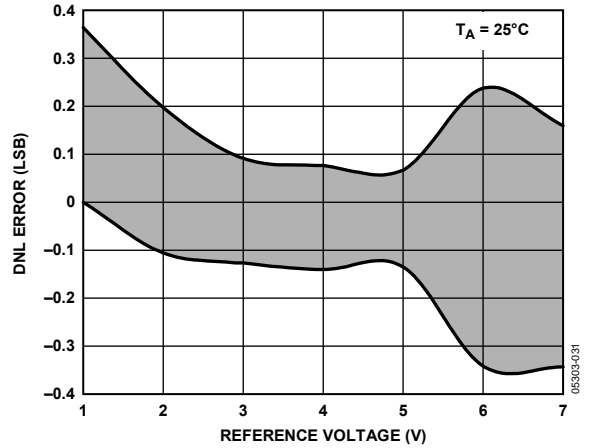


Figure 18. Differential Nonlinearity Error vs. Reference Voltage,  $AV_{DD}/AV_{SS} = \pm 16.5V$

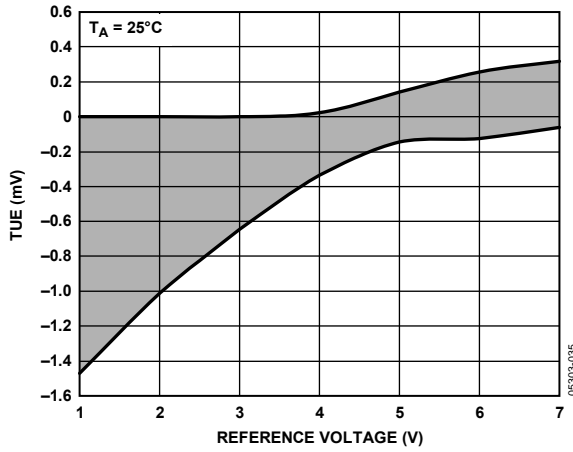


Figure 19. Total Unadjusted Error vs. Reference Voltage,  $AV_{DD}/AV_{SS} = \pm 16.5\text{ V}$

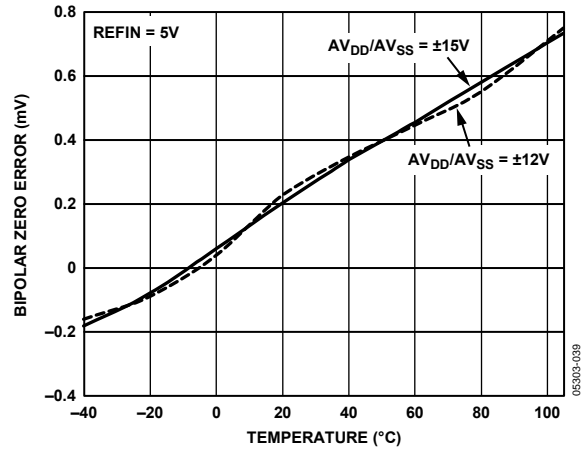


Figure 22. Bipolar Zero Error vs. Temperature

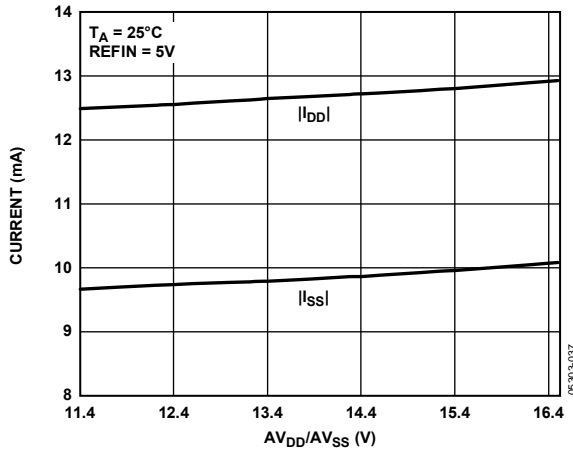


Figure 20.  $I_{DD}/I_{SS}$  vs.  $AV_{DD}/AV_{SS}$

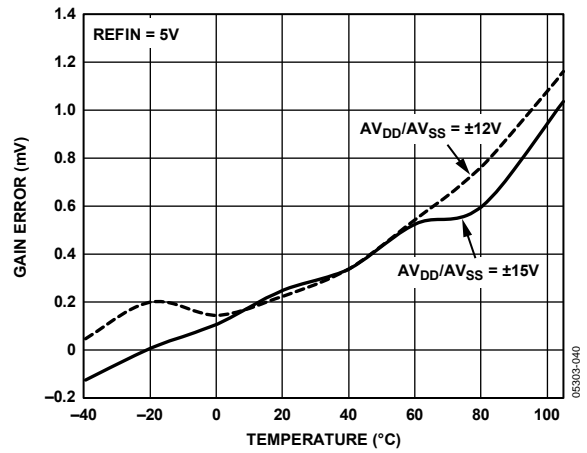


Figure 23. Gain Error vs. Temperature

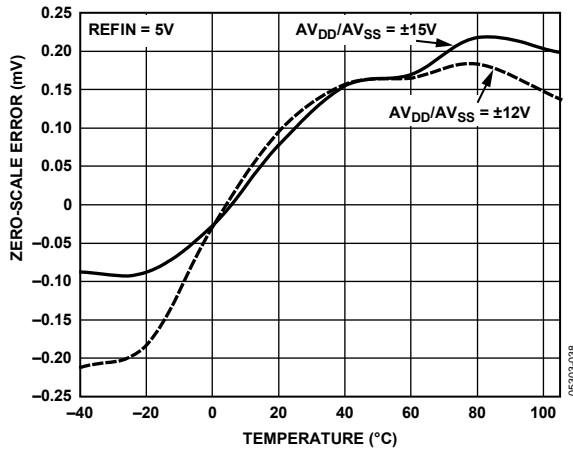


Figure 21. Zero-Scale Error vs. Temperature

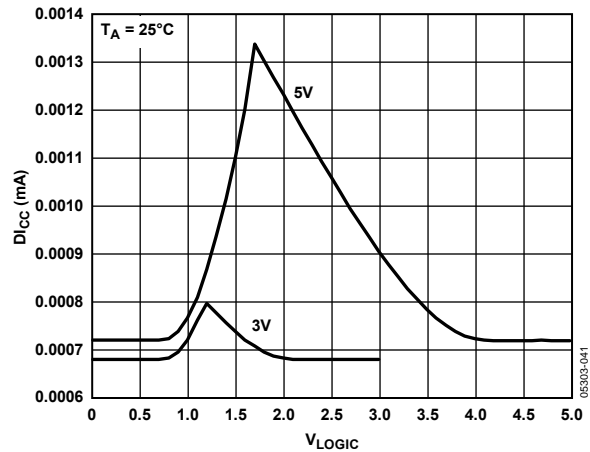


Figure 24.  $D_{ICC}$  vs. Logic Input Voltage

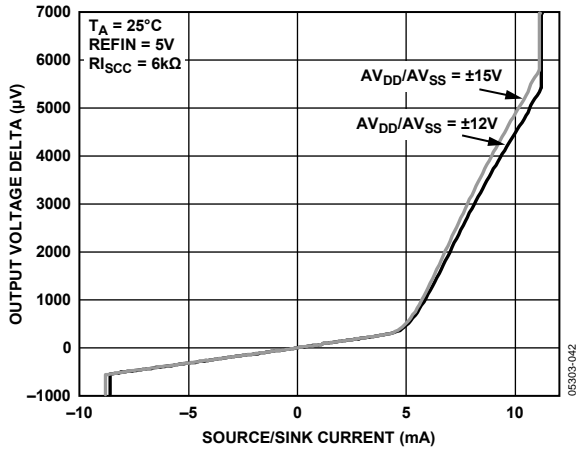


Figure 25. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

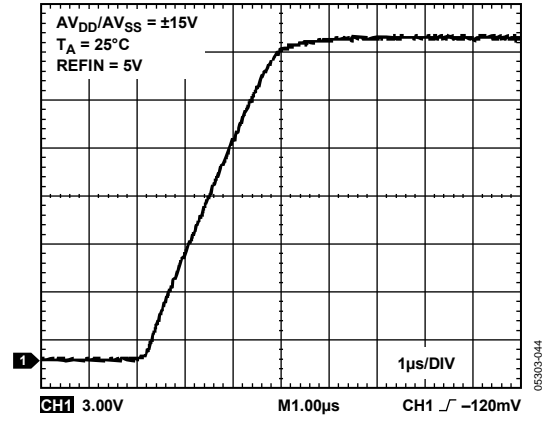


Figure 27. Full-Scale Settling Time

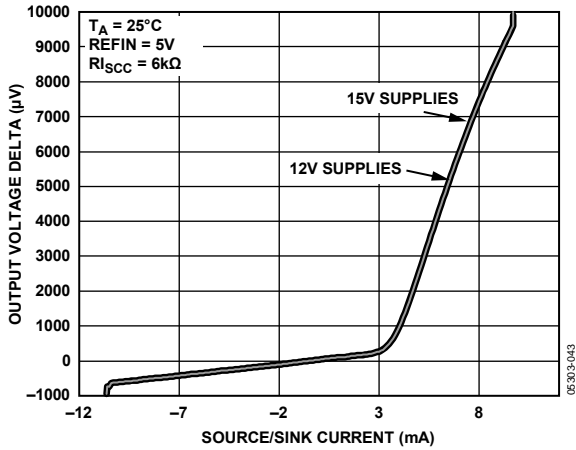


Figure 26. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

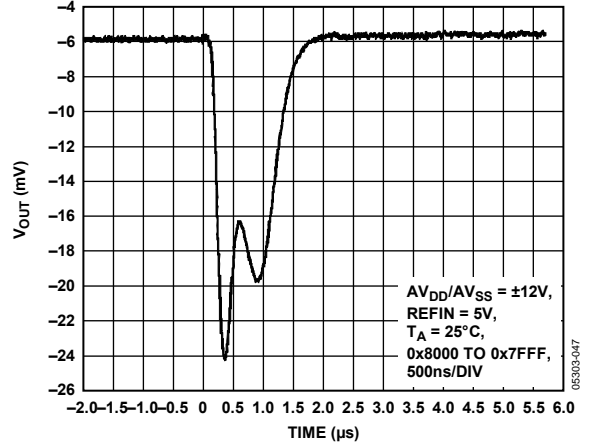


Figure 28. Major Code Transition Glitch Energy,  $AV_{DD}/AV_{SS} = \pm 12\text{V}$

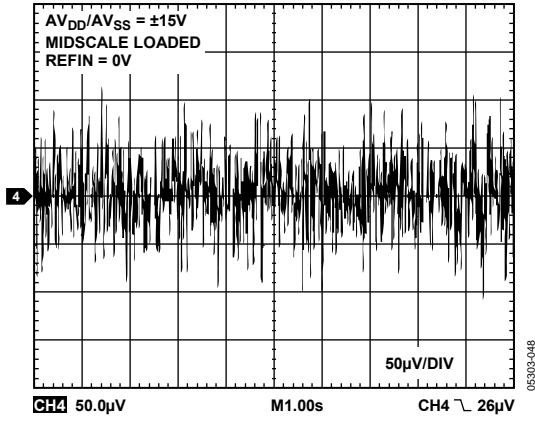


Figure 29. Peak-to-Peak Noise (100 kHz Bandwidth)

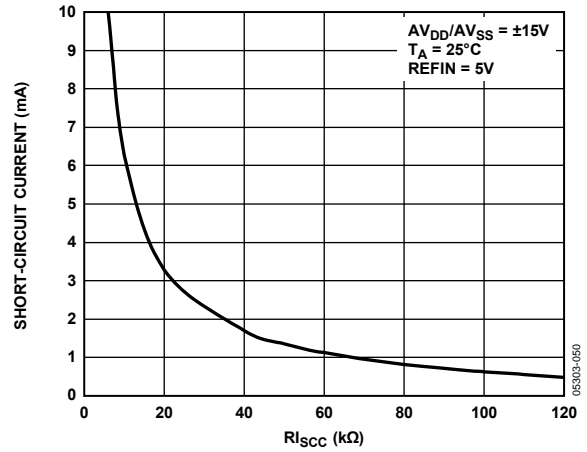


Figure 31. Short-Circuit Current vs. RL<sub>SCC</sub>

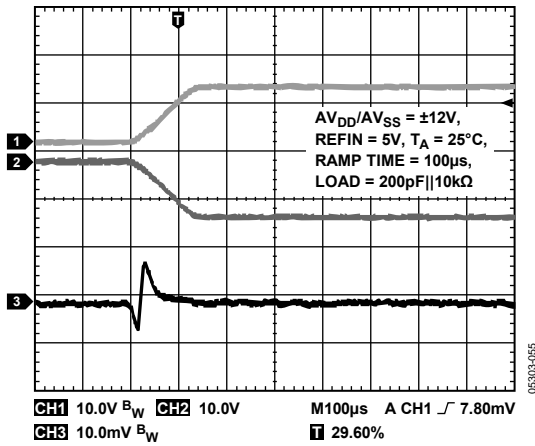


Figure 30. V<sub>OUT</sub> vs. AV<sub>DD</sub>/AV<sub>SS</sub> on Power-Up



## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 7.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic. A typical DNL vs. code plot can be seen in Figure 9.

### Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5764 is monotonic over its full operating temperature range.

### Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (offset binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 22.

### Bipolar Zero Temperature Coefficient (TC)

Bipolar zero TC is the measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/ $^{\circ}$ C.

### Full-Scale Error

Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output voltage should be  $2 \times V_{REF} - 1$  LSB. Full-scale error is expressed in percentage of full-scale range.

### Negative Full-Scale Error/Zero-Scale Error

Negative full-scale error is the error in the DAC output voltage when 0x0000 (offset binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be  $-2 \times V_{REF}$ . A plot of zero-scale error vs. temperature can be seen in Figure 21.

### Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

### Slew Rate

The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/ $\mu$ s.

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range. A plot of gain error vs. temperature can be seen in Figure 23.

### Total Unadjusted Error

Total unadjusted error (TUE) is a measure of the output error considering all the various errors. A plot of total unadjusted error vs. reference can be seen in Figure 19.

### Zero-Scale Error Temperature Coefficient (TC)

Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/ $^{\circ}$ C.

### Gain Error Temperature Coefficient (TC)

Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in (ppm of FSR)/ $^{\circ}$ C.

### Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000), see Figure 28.

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-secs and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

### Power Supply Sensitivity

Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

### DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, and is expressed in LSBs.

### DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with LDAC low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

### Channel-to-Channel Isolation

Channel-to-channel isolation is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

### Digital Crosstalk

Digital crosstalk is a measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC but is measured when the DAC output is not updated. It is specified in nV-secs and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

## THEORY OF OPERATION

The AD5764 is a quad, 16-bit, serial input, bipolar voltage output DAC and operates from supply voltages of  $\pm 11.4$  V to  $\pm 16.5$  V and has a buffered output voltage of up to  $\pm 10.5263$  V. Data is written to the AD5764 in a 24-bit word format, via a 3-wire serial interface. The device also offers an SDO pin, which is available for daisy-chaining or readback.

The AD5764 incorporates a power-on reset circuit, which ensures that the DAC registers power up loaded with 0x0000. The AD5764 features a digital I/O port that can be programmed via the serial interface, on-chip reference buffers and per channel digital gain, and offset registers.

### DAC ARCHITECTURE

The DAC architecture of the AD5764 consists of a 16-bit current mode segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 32.

The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGND<sub>x</sub> or IOU<sub>T</sub>. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of the 12-bit R-2R ladder network.

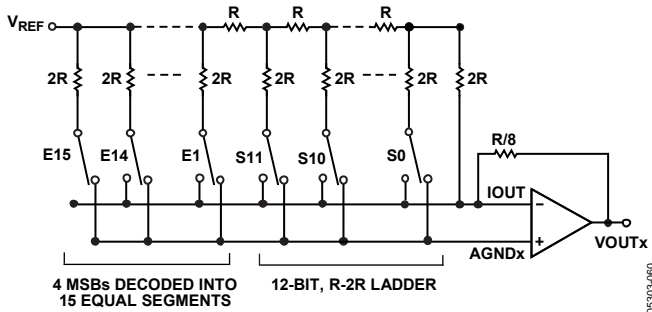


Figure 32. DAC Ladder Structure

### REFERENCE BUFFERS

The AD5764 operates with an external reference. The reference inputs (REFAB and REFC<sub>D</sub>) have an input range up to 7 V. This input voltage is used to provide a buffered positive and negative reference for the DAC cores. The positive reference is given by

$$+V_{REF} = 2 \times V_{REF}$$

The negative reference to the DAC cores is given by

$$-V_{REF} = -2 \times V_{REF}$$

These positive and negative reference voltages (along with the gain register values) define the output ranges of the DACs.

### SERIAL INTERFACE

The AD5764 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

#### Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, three register select bits, three DAC address bits, and 16 data bits, as shown in Table 8. The timing diagram for this operation is shown in Figure 2.

Upon power-up, the DAC registers are loaded with zero code (0x0000), and the outputs are clamped to 0 V via a low impedance path. The outputs can be updated with the zero code value at this time by asserting either LDAC or CLR. The corresponding output voltage depends on the state of the BIN/2sCOMP pin. If the BIN/2sCOMP pin is tied to DGND, the data coding is twos complement, and the outputs update to 0 V. If the BIN/2sCOMP pin is tied to DV<sub>CC</sub>, the data coding is offset binary, and the outputs update to negative full scale. To have the outputs power-up with zero code loaded to the outputs, the CLR pin should be held low during power-up.

#### Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and SYNC must be taken high after the final clock to latch the data. The first falling edge of SYNC starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before SYNC is brought high again. If SYNC is brought high before the 24<sup>th</sup> falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before SYNC is brought high, the input data is also invalid. The input register addressed is updated on the rising edge of SYNC. For another serial transfer to take place, SYNC must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, all DAC registers and outputs can be updated by taking LDAC low.

### Daisy-Chain Operation

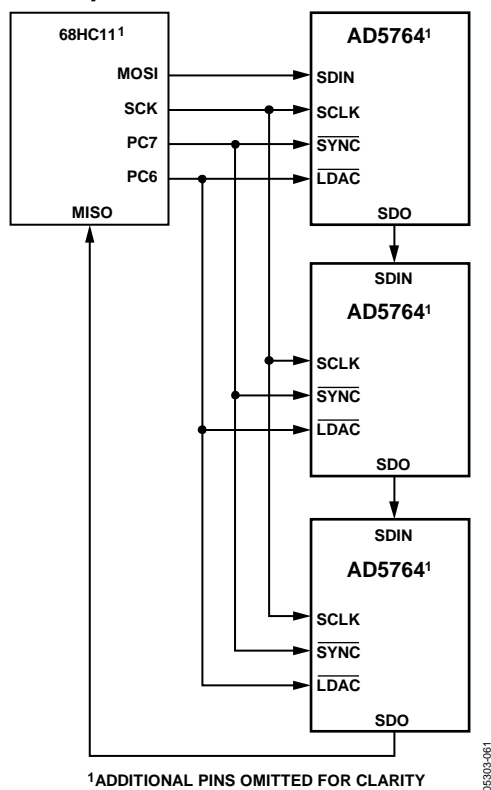


Figure 33. Daisy-Chaining the AD5764

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of  $\overline{\text{SYNC}}$  starts the write cycle. The  $\overline{\text{SCLK}}$  is continuously applied to the input shift register when  $\overline{\text{SYNC}}$  is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of  $\overline{\text{SCLK}}$  and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal  $24N$ , where  $N$  is the total number of AD5764 devices in the chain. When the serial transfer to all devices is complete,  $\overline{\text{SYNC}}$  is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or a gated clock.

A continuous  $\overline{\text{SCLK}}$  source can only be used if  $\overline{\text{SYNC}}$  is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and  $\overline{\text{SYNC}}$  must be taken high after the final clock to latch the data.

### Readback Operation

Before a readback operation is initiated, the SDO pin must be enabled by writing to the function register and clearing the SDO

disable bit; this bit is cleared by default. Readback mode is invoked by setting the  $\overline{\text{R/W}}$  bit = 1 in the serial input register write. With  $\overline{\text{R/W}} = 1$ , Bit A2 to Bit A0, in association with Bit REG2, Bit REG1, and Bit REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output contain the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the fine gain register of Channel A on the AD5764, implement the following:

1. Write  $0xA0XXXX$  to the AD5764 input register. This configures the AD5764 for read mode with the fine gain register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't cares.
2. Follow this with a second write, an NOP condition,  $0x00XXXX$ . During this write, the data from the fine gain register is clocked out on the SDO line, that is, data clocked out contain the data from the fine gain register in Bit DB5 to Bit DB0.

### SIMULTANEOUS UPDATING VIA $\overline{\text{LDAC}}$

Depending on the status of both  $\overline{\text{SYNC}}$  and  $\overline{\text{LDAC}}$ , and after data has been transferred into the input register of the DACs, there are two ways in which the DAC registers and DAC outputs can be updated.

#### Individual DAC Updating

In this mode,  $\overline{\text{LDAC}}$  is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of  $\overline{\text{SYNC}}$ .

#### Simultaneous Updating of All DACs

In this mode,  $\overline{\text{LDAC}}$  is held high while data is being clocked into the input shift register. All DAC outputs are updated by taking  $\overline{\text{LDAC}}$  low any time after  $\overline{\text{SYNC}}$  has been taken high. The update now occurs on the falling edge of  $\overline{\text{LDAC}}$ .

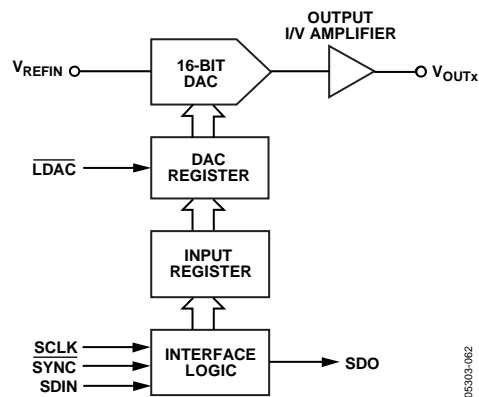


Figure 34. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel

# AD5764

## TRANSFER FUNCTION

Table 7 shows the ideal input code to output voltage relationship for the AD5764 for both offset binary and twos complement data coding.

**Table 7. Ideal Output Voltage to Input Code Relationship**

Digital Input				Analog Output
Offset Binary Data Coding				
MSB	LSB			VOUTx
1111	1111	1111	1111	+2 V <sub>REF</sub> × (32,767/32,768)
1000	0000	0000	0001	+2 V <sub>REF</sub> × (1/32,768)
1000	0000	0000	0000	0 V
0111	1111	1111	1111	-2 V <sub>REF</sub> × (1/32,768)
0000	0000	0000	0000	-2 V <sub>REF</sub> × (32,767/32,768)
Twos Complement Data Coding				VOUTx
MSB	LSB			
0111	1111	1111	1111	+2 V <sub>REF</sub> × (32,767/32,768)
0000	0000	0000	0001	+2 V <sub>REF</sub> × (1/32,768)
0000	0000	0000	0000	0 V
1111	1111	1111	1111	-2 V <sub>REF</sub> × (1/32,768)
1000	0000	0000	0000	-2 V <sub>REF</sub> × (32,767/32,768)

The output voltage expression for the AD5764 is given by

$$V_{OUT} = -2 \times V_{REFIN} + 4 \times V_{REFIN} \left[ \frac{D}{65,536} \right]$$

where:

$D$  is the decimal equivalent of the code loaded to the DAC.

$V_{REFIN}$  is the reference voltage applied at the REFAB/REFCD pins.

## ASYNCHRONOUS CLEAR ( $\overline{\text{CLR}}$ )

$\overline{\text{CLR}}$  is a negative edge triggered clear that allows the outputs to be cleared to either 0 V (twos complement coding) or negative full scale (offset binary coding). It is necessary to maintain  $\overline{\text{CLR}}$  low for a minimum amount of time (see Figure 2) for the operation to complete. When the  $\overline{\text{CLR}}$  signal is returned high, the output remains at the cleared value until a new value is programmed. If at power-on,  $\overline{\text{CLR}}$  is at 0 V, then all DAC outputs are updated with the clear value. A clear can also be initiated through software by writing the command 0x04XXXX to the AD5764.

**Table 8. Input Register Bit Map**

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15:DB0
R/W	0	REG2	REG1	REG0	A2	A1	A0	DATA

**Table 9. Input Register Bit Functions**

Bit	Description			
R/W	Indicates a read from or a write to the addressed register.			
REG2, REG1, REG0	Used in association with the address bits to determine if a read or write operation is to the data register, offset register, gain register, or function register.			
	REG2	REG1	REG0	Function
	0	0	0	Function Register
	0	1	0	Data Register
	0	1	1	Coarse Gain Register
	1	0	0	Fine Gain Register
	1	0	1	Offset Register
A2, A1, A0	These bits are used to decode the DAC channels.			
	A2	A1	A0	Channel Address
	0	0	0	DAC A
	0	0	1	DAC B
	0	1	0	DAC C
	0	1	1	DAC D
	1	0	0	All DACs
D15:D0	Data Bits.			

## FUNCTION REGISTER

The function register is addressed by setting the three REG bits to 000. The values written to the address bits and the data bits determine the function addressed. The functions available via the function register are outlined in Table 10 and Table 11.

**Table 10. Function Register Options**

REG2	REG1	REG0	A2	A1	A0	DB15:DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	NOP, Data = Don't Care						
0	0	0	0	0	1	Don't Care	Local-Ground-Offset Adjust	D1 Direction	D1 Value	D0 Direction	D0 Value	SDO Disable
0	0	0	1	0	0	CLR, Data = Don't Care						
0	0	0	1	0	1	LOAD, Data = Don't Care						

**Table 11. Explanation of Function Register Options**

Option	Description
NOP	No operation instruction used in readback operations.
Local-Ground-Offset Adjust	Set by the user to enable local-ground-offset adjust function. Cleared by the user to disable local-ground-offset adjust function (default). Refer to the Design Features section for further details.
D0/D1 Direction	Set by the user to enable D0/D1 as outputs. Cleared by the user to enable D0/D1 as inputs (default). Refer to the Design Features section for further details.
D0/D1 Value	I/O Port Status Bits. Logic values written to these locations determine the logic outputs on the D0 and D1 pins when configured as outputs. These bits indicate the status of the D0 and D1 pins when the I/O port is active as an input. When enabled as inputs, these bits are don't cares during a write operation.
SDO Disable	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
CLR	Addressing this function resets the DAC outputs to 0V in twos complement mode and negative full scale in binary mode.
LOAD	Addressing this function updates the DAC registers and consequently the analog outputs.

## DATA REGISTER

The data register is addressed by setting the three REG bits to 010. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). Position the data bits from DB15 to DB0, as shown in Table 12.

**Table 12. Programming the Data Register Bit Map**

REG2	REG1	REG0	A2	A1	A0	DB15:DB0
0	1	0	DAC Address			16-Bit DAC Data

## COARSE GAIN REGISTER

The coarse gain register is addressed by setting the three REG bits to 011. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The coarse gain register is a 2-bit register and allows the user to select the output range of each DAC, as shown in Table 13 and Table 14.

**Table 13. Programming the Coarse Gain Register Bit Map**

REG2	REG1	REG0	A2	A1	A0	DB15:DB2	DB1	DB0
0	1	1	DAC Address			Don't Care	CG1	CG0

**Table 14. Output Range Selection**

Output Range	CG1	CG0
±10 V (Default)	0	0
±10.2564 V	0	1
±10.5263 V	1	0

# AD5764

## FINE GAIN REGISTER

The fine gain register is addressed by setting the three REG bits to 100. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The fine gain register is a 6-bit register and allows the user to adjust the gain

of each DAC channel by  $-32$  LSBs to  $+31$  LSBs in 1 LSB increments, as shown in Table 15 and Table 16. The adjustment is made to both the positive full-scale points and the negative full-scale points simultaneously, each point being adjusted by  $\frac{1}{2}$  of one step. The fine gain register coding is twos complement.

**Table 15. Programming the Fine Gain Register Bit Map**

REG2	REG1	REG0	A2	A1	A0	DB15:DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	DAC Address			Don't Care	FG5	FG4	FG3	FG2	FG1	FG0

**Table 16. AD5764 Fine Gain Register Options**

Gain Adjustment	FG5	FG4	FG3	FG2	FG1	FG0
+31 LSBs	0	1	1	1	1	1
+30 LSBs	0	1	1	1	1	0
...	...	...	...	...	...	...
+2 LSBs	0	0	0	0	1	0
+1 LSB	0	0	0	0	0	1
No Adjustment (Default)	0	0	0	0	0	0
-1 LSB	1	1	1	1	1	1
-2 LSBs	1	1	1	1	1	0
...	...	...	...	...	...	...
-31 LSBs	1	0	0	0	0	1
-32 LSBs	1	0	0	0	0	0

**OFFSET REGISTER**

The offset register is addressed by setting the three REG bits to 101. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The AD5764 offset

register is an 8-bit register and allows the user to adjust the offset of each channel by  $-16$  LSBs to  $+15.875$  LSBs in increments of  $\frac{1}{8}$  LSB, as shown in Table 17 and Table 18. The offset register coding is twos complement.

**Table 17. Programming the Offset Register Bit Map**

REG2	REG1	REG0	A2	A1	A0	DB15:DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	DAC Address			Don't Care	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

**Table 18. AD5764 Offset Register Options**

Offset Adjustment	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
+15.875 LSBs	0	1	1	1	1	1	1	1
+15.75 LSBs	0	1	1	1	1	1	1	0
...	...	...	...	...	...	...	...	...
+0.25 LSBs	0	0	0	0	0	0	1	0
+0.125 LSBs	0	0	0	0	0	0	0	1
No Adjustment (Default)	0	0	0	0	0	0	0	0
-0.125 LSBs	1	1	1	1	1	1	1	1
-0.25 LSBs	1	1	1	1	1	1	1	0
...	...	...	...	...	...	...	...	...
-15.875 LSBs	1	0	0	0	0	0	0	1
-16 LSBs	1	0	0	0	0	0	0	0

## OFFSET AND GAIN ADJUSTMENT WORKED EXAMPLE

Using the information provided in the previous section, the following worked example demonstrates how the AD5764 functions can be used to eliminate both offset and gain errors. Because the AD5764 is factory calibrated, offset and gain errors should be negligible. However, errors can be introduced by the system that the AD5764 is operating within, for example, a voltage reference value that is not equal to 5 V introduces a gain error. An output range of  $\pm 10$  V and twos complement data coding is assumed.

### Removing Offset Error

The AD5764 can eliminate an offset error in the range of  $-4.88$  mV to  $+4.84$  mV with a step size of  $\frac{1}{8}$  of a 16-bit LSB.

Calculate the step size of the offset adjustment.

$$\text{Offset Adjust Step Size} = \frac{20}{2^{16} \times 8} = 38.14 \mu\text{V}$$

Measure the offset error by programming 0x0000 to the data register and measuring the resulting output voltage, for this example the measured value is  $614 \mu\text{V}$ .

Calculate the number of offset adjustment steps that this value represents.

$$\text{Number of Steps} = \frac{\text{Measured Offset Value}}{\text{Offset Step Size}} = \frac{614 \mu\text{V}}{38.14 \mu\text{V}} = 16 \text{ Steps}$$

The offset error measured is positive, therefore, a negative adjustment of 16 steps is required. The offset register is 8 bits wide and the coding is twos complement. The required offset register value can be calculated as follows:

Convert adjustment value to binary: 00010000.

Convert this to a negative twos complement number by inverting all bits and adding 1: 11110000.

11110000 is the value that should be programmed to the offset register.

Note that this twos complement conversion is not necessary in the case of a positive offset adjustment. The value to be programmed to the offset register is simply the binary representation of the adjustment value.

### Removing Gain Error

The AD5764 can eliminate a gain error at negative full-scale output in the range of  $-9.77$  mV to  $+9.46$  mV with a step size of  $\frac{1}{2}$  of a 16-bit LSB.

Calculate the step size of the gain adjustment.

$$\text{Gain Adjust Step Size} = \frac{20}{2^{16} \times 2} = 152.59 \mu\text{V}$$

Measure the gain error by programming 0x8000 to the data register and measuring the resulting output voltage. The gain error is the difference between this value and  $-10$  V; for this example, the gain error is  $-1.2$  mV.

Calculate how many gain adjustment steps this value represents.

$$\text{Number of Steps} = \frac{\text{Measured Gain Value}}{\text{Gain Step Size}} = \frac{1.2 \text{ mV}}{152.59 \mu\text{V}} = 8 \text{ Steps}$$

The gain error measured is negative (in terms of magnitude); therefore, a positive adjustment of eight steps is required. The gain register is 6 bits wide and the coding is twos complement, the required gain register value can be determined as follows: Convert adjustment value to binary: 001000.

The value to be programmed to the gain register is simply this binary number.



## DESIGN FEATURES

### ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power-up and during brownout conditions. When the supply voltages are changing, the VOUTx pins are clamped to 0 V via a low impedance path. To prevent the output amp being shorted to 0 V during this time, Transmission Gate G1 is also opened (see Figure 35). These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the reset logic (RSTIN) control input. For instance, if  $\overline{\text{RSTIN}}$  is driven from a battery supervisor chip, the  $\overline{\text{RSTIN}}$  input is driven low to open G1 and close G2 on power-down or during a brownout. Conversely, the on-chip voltage detector output ( $\overline{\text{RSTOUT}}$ ) is also available to the user to control other parts of the system. The basic transmission gate functionality is shown in Figure 35.

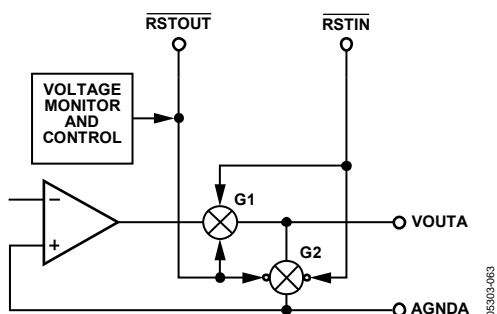


Figure 35. Analog Output Control Circuitry

### DIGITAL OFFSET AND GAIN CONTROL

The AD5764 incorporates a digital offset adjust function with a  $\pm 16$  LSB adjust range and 0.125 LSB resolution. The gain register allows the user to adjust the AD5764 full-scale output range. The full-scale output can be programmed to achieve full-scale ranges of  $\pm 10$  V,  $\pm 10.25$  V, and  $\pm 10.5$  V. A fine gain trim is also provided.

### PROGRAMMABLE SHORT-CIRCUIT PROTECTION

The short-circuit current of the output amplifiers can be programmed by inserting an external resistor between the ISCC pin and PGND. The programmable range for the current is 500  $\mu\text{A}$  to 10 mA, corresponding to a resistor range of 120 k $\Omega$  to 6 k $\Omega$ . The resistor value is calculated as follows:

$$R = \frac{60}{I_{\text{SC}}}$$

If the ISCC pin is left unconnected, the short-circuit current limit defaults to 5 mA. Note that limiting the short-circuit current to a small value can affect the slew rate of the output when driving into a capacitive load; therefore, the value of the programmed short-circuit should take into account the size of the capacitive load being driven.

### DIGITAL I/O PORT

The AD5764 contains a 2-bit digital I/O port (D1 and D0). These bits can be configured as inputs or outputs independently, and can be driven or have their values read back via the serial interface. The I/O port signals are referenced to DV<sub>CC</sub> and DGND. When configured as outputs, they can be used as control signals to multiplexers or can be used to control calibration circuitry elsewhere in the system. When configured as inputs, the logic signals from limit switches can, for example, be applied to D0 and D1 and can be read back via the digital interface.

### LOCAL GROUND OFFSET ADJUST

The AD5764 incorporates a local-ground-offset adjust feature that, when enabled in the function register, adjusts the DAC outputs for voltage differences between the individual DAC ground pins and the REFGND pin ensuring that the DAC output voltages are always with respect to the local DAC ground pin. For instance, if pin AGNDA is at +5 mV with respect to the REFGND pin and VOUTA is measured with respect to AGNDA, a  $-5$  mV error results, enabling the local-ground-offset adjust feature to adjust VOUTA by +5 mV, eliminating the error.

## APPLICATIONS INFORMATION

### TYPICAL OPERATING CIRCUIT

Figure 36 shows the typical operating circuit for the AD5764. The only external components needed for this precision 16-bit DAC are a reference voltage source, decoupling capacitors on the supply pins and reference inputs, and an optional short-circuit current setting resistor. Because the device incorporates reference buffers, it eliminates the need for an external bipolar

reference and associated buffers. This leads to an overall savings in both cost and board space.

In Figure 36,  $AV_{DD}$  is connected to +15 V and  $AV_{SS}$  is connected to -15 V. However,  $AV_{DD}$  can operate with supplies from +11.4 V to +16.5 V and  $AV_{SS}$  can operate with supplies from -11.4 V to -16.5 V.

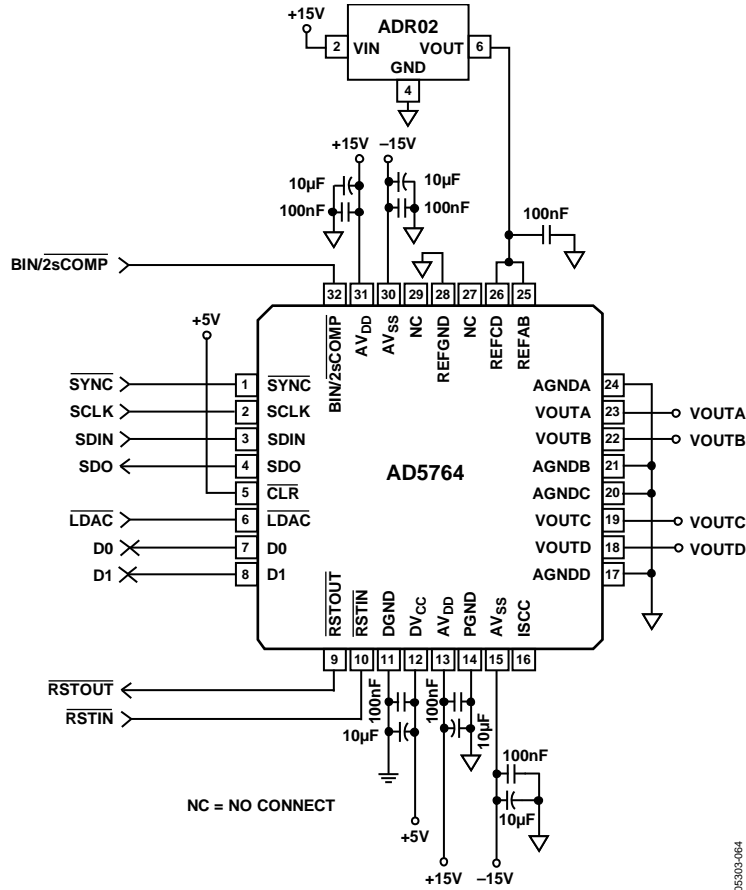


Figure 36. Typical Operating Circuit

05303-064

### Precision Voltage Reference Selection

To achieve the optimum performance from the AD5764 over its full operating temperature range, a precision voltage reference must be used. Thought should be given to the selection of a precision voltage reference. The AD5764 has two reference inputs, REFAB and REFC. The voltages applied to the reference inputs are used to provide a buffered positive and negative reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference could lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the [ADR425](#), allows a system designer to trim system errors out by setting the reference

voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the [ADR435](#) (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

**Table 19. Some Precision References Recommended for Use with the AD5764**

Part No.	Initial Accuracy (mV Max)	Long-Term Drift (ppm Typ)	Temp Drift (ppm/°C Max)	0.1 Hz to 10 Hz Noise (μV p-p Typ)
<a href="#">ADR435</a>	±6	30	3	3.4
<a href="#">ADR425</a>	±6	50	3	3.4
<a href="#">ADR02</a>	±5	50	3	15
<a href="#">ADR395</a>	±6	50	25	5
<a href="#">AD586</a>	±2.5	15	10	4

## LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5764 is mounted must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5764 is in a system where multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device. The AD5764 is to have ample supply bypassing of 10  $\mu\text{F}$  in parallel with 0.1  $\mu\text{F}$  on each supply located as close to the package as possible, ideally right up against the device. The 10  $\mu\text{F}$  capacitors are the tantalum bead type. The 0.1  $\mu\text{F}$  capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5764 are to be as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, are to be shielded with digital ground to avoid radiating noise to other parts of the board, and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane, however, it is helpful to separate the lines). It is essential to minimize noise on the reference inputs, because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board are to run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, and signal traces are placed on the solder side.

## GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. Isocouplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5764 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 37 shows a 4-channel isolated interface to the AD5764 using an ADuM1400. For more information, go to [www.analog.com](http://www.analog.com).

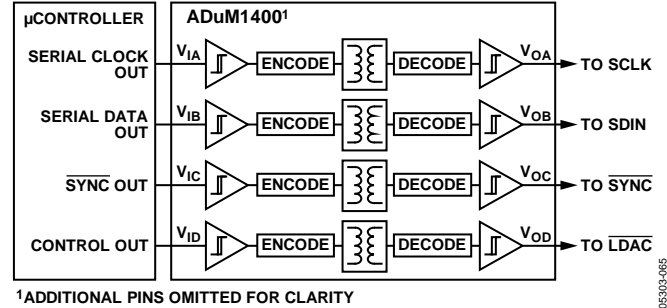


Figure 37. Isolated Interface

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5764 is via a serial bus that uses a standard protocol that is compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5764 requires a 24-bit data-word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update can be done automatically when all the data is clocked in, or it can be done under the control of LDAC. The contents of the DAC register can be read using the readback function.

### AD5764 to MC68HC11 Interface

Figure 38 shows an example of a serial interface between the AD5764 and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), clock polarity bit (CPOL = 0), and the clock phase bit (CPHA = 1). The SPI is configured by writing to the SPI control register (SPCR) (see the *MC68HC11 User Manual*). SCK of the MC68HC11 drives the SCLK of the AD5764, the MOSI output drives the serial data line (DIN) of the AD5764, and the MISO input is driven from SDO. The SYNC is driven from one of the port lines, in this case, PC7.

When data is being transmitted to the AD5764, the SYNC line (PC7) is taken low and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle, therefore, to load the required 24-bit word, PC7 is not brought high until the third 8-bit word has been transferred to the DAC input shift register.

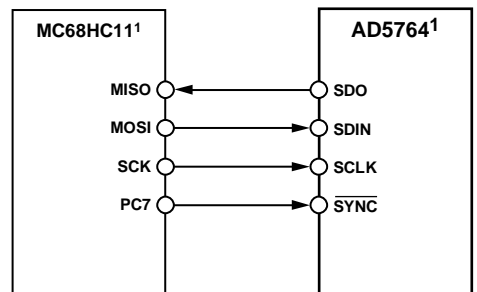


Figure 38. AD5764 to MC68HC11 Interface.

$\overline{\text{LDAC}}$  is controlled by the PC6 port output. The DAC can be updated after each 3-byte transfer by bringing  $\overline{\text{LDAC}}$  low. This example does not show other serial lines for the DAC. For example, if  $\overline{\text{CLR}}$  were used, it could be controlled by Port Output PC5.

### AD5764 to 8XC51 Interface

The AD5764 requires a clock synchronized to the serial data. For this reason, the 8XC51 must be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on TxD.

P3.3 and P3.4 are bit programmable pins on the serial port and are used to drive  $\overline{\text{SYNC}}$  and  $\overline{\text{LDAC}}$ , respectively. The 8XC51 provides the LSB of its SBUF register as the first bit in the data stream. The user must ensure that the data in the SBUF register is arranged correctly, because the DAC expects the MSB first. When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge. As a result, no glue logic is required between this DAC and the microcontroller interface.

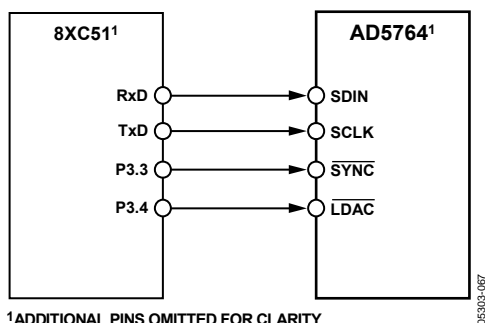


Figure 39. AD5764 to 8XC51 Interface

The 8XC51 transmits data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Because the DAC expects a 24-bit word,  $\overline{\text{SYNC}}$  (P3.3) must be left low after the first eight bits are transferred. After the third byte has been transferred, the P3.3 line is taken high. The DAC can be updated using  $\overline{\text{LDAC}}$  via P3.4 of the 8XC51.

### AD5764 to ADSP-2101 Interface

An interface between the AD5764 and the ADSP-2101 is shown in Figure 40. The ADSP-2101 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101 is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 24-bit word length.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the DAC. In the interface shown, the DAC

output is updated using the  $\overline{\text{LDAC}}$  pin via the DSP. Alternatively, the  $\overline{\text{LDAC}}$  input can be tied permanently low, and then the update takes place automatically when TFS is taken high.

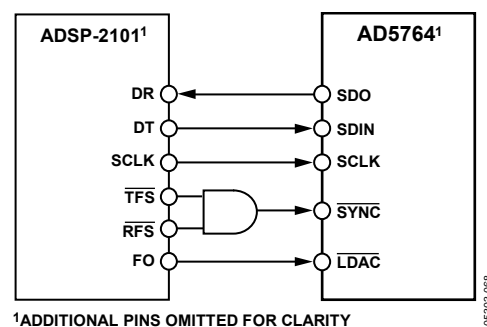


Figure 40. AD5764 to ADSP-2101 Interface.

### AD5764 to PIC16C6x/PIC16C7x Interface

The PIC16C6x/PIC16C7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit set to 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example, I/O Port RA1 is being used to pulse  $\overline{\text{SYNC}}$  and enable the serial port of the AD5764. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are needed. Figure 41 shows the connection diagram.

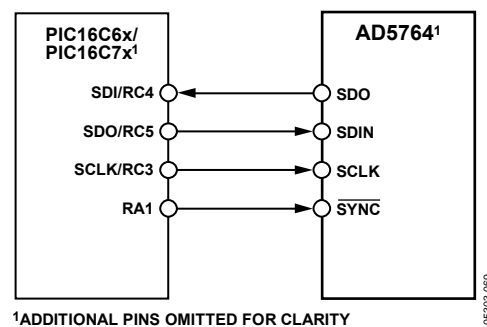


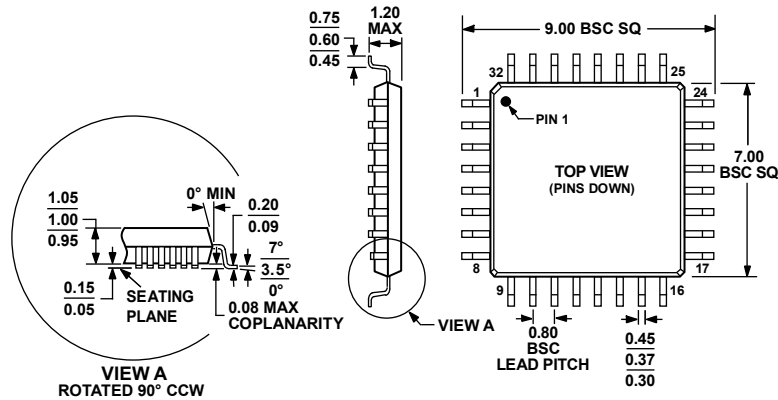
Figure 41. AD5764 to PIC16C6x/PIC16C7x Interface

## EVALUATION BOARD

The AD5764 comes with a full evaluation board to aid designers in evaluating the high performance of the part with minimum effort. All that is required with the evaluation board is a power supply and a PC. The AD5764 evaluation kit includes a populated, tested AD5764 PCB. The evaluation board interfaces to the USB port of the PC. Software is available with the evaluation board, which allows the user to easily program the AD5764. The software runs on any PC that has Microsoft® Windows® 2000/NT/XP installed.

The [EVAL-AD5764EB](#) data sheet is available, which gives full details on operating the evaluation board.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ABA

Figure 42. 32-Lead Thin Plastic Quad Flat Package [TQFP] (SU-32-2)

Dimensions shown in millimeters

020607-A

## ORDERING GUIDE

Model	INL	Temperature Range	Package Description	Package Option
AD5764ASUZ <sup>1</sup>	±4 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
AD5764ASUZ-REEL7 <sup>1</sup>	±4 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
AD5764BSUZ <sup>1</sup>	±2 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
AD5764BSUZ-REEL7 <sup>1</sup>	±2 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
AD5764CSUZ <sup>1</sup>	±1 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
AD5764CSUZ-REEL7 <sup>1</sup>	±1 LSB max	-40°C to +85°C	32-Lead TQFP	SU-32-2
EVAL-AD5764EBZ <sup>1</sup>			Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**AD5764**

**NOTES**